REMARKS

Claims 1-37 are currently pending in the application. Claims 1, 11-13, 15, 18-24, 27, 29, and 31-37 were rejected. Claims 2-10, 14, 16, 17, 25, 26, 28, and 30 were objected to.

The Examiner objected to claims 5 and 8 for the same reason. The Applicants respectfully point out that the claims are correct in their current form and that the proposed amendment should not be entered. That is, both of these claims recite "a synchronous handshake with the particular clock domain." This handshake is synchronous in nature, i.e., it is clock dependent, and is in addition to the asynchronous handshake protocol recited. In view of the foregoing, the objection is believed addressed.

The Examiner rejected claims 1, 11-13, 15, 18, 20, and 27 under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,546,451 (Venkataraman) in view of U.S. Patent No. 6,112,016 (MacWilliams) and U.S. Patent No. 5,875,338 (Powell). The Examiner also rejected claims 19, 21-24, 27, 29, and 31-37 over these three references in combination with a variety of other references. The rejection is respectfully traversed.

Venkataraman describes a node controller in which the processor speed is decoupled from the memory subsystem speed (see Abstract and Technical Field of the Invention). Node controller 12 mediates communication among network 14, processor 16, memory 17, and I/O device 18 (see FIG. 1 and corresponding description). Node controller 12 employs a crossbar unit 30 to pass data among these node components via corresponding interfaces 20, 24, 22, and 26 (see FIG. 2 and the corresponding description).

As the Examiner points out, Venkataraman notes that "[t]here may be asynchronous boundaries between processor interface unit 24 and crossbar unit 30 and between input/output interface unit 26 and crossbar unit 30." (col. 3, lines 17-19) What the Examiner fails to point out, however, is that "[t]his asynchronous boundary occurs as a result of a core clock driving crossbar unit 30 being at a different non-integer clock ratio clock speed than the clock speed of

processor interface unit 24 and its associated processor 16 or input/output interface unit 26 and its associated input/output device 18." (col. 3, lines 19-24) That is, crossbar unit 30 is a synchronous unit because it has its own clock which controls its operation. As a result, "data entering crossbar unit 30 from either processor interface unit 24 or input/output interface unit 26 needs to be synchronized to the core clock speed of crossbar unit 30." (col. 3, lines 24-27).

Thus, contrary to the Examiner's assertion, crossbar unit 30 does not "operate in the asynchronous domain." Rather, because data entering synchronous crossbar unit 30 needs to be synchronized with its core clock, the solution offered by Venkataraman suffers from the same disadvantages described in the Background of the Invention of the present application with regard to the example of the high speed bus interconnecting system components having different clock speeds. The Examiner has misinterpreted Venkataraman's use of the term "asynchronous" with respect to the boundaries between system components. Use of this term in this context merely refers to the fact that some synchronization is required at these interfaces due to the differing clock speeds of the connecting components. It clearly does not apply to crossbar unit 30 or its manner of operation.

By contrast and as recited in claim 1, the present invention provides "an asynchronous crossbar coupled to the plurality of clock domain converters, and operable in the asynchronous domain to implement a first-in-first-out (FIFO) channel between any two of the clock domain converters, thereby facilitating communication between any two of the synchronous modules." As described in the present specification, the clock domain converters in combination with the asynchronous nature of this crossbar "allow the high-speed interconnection of disparate clock domains while simultaneously *eliminating issues relating to synchronization of the various data rates*." (Emphasis added; see page 85, lines 2-3). "In addition, because of the asynchronous nature of the interconnect, the various synchronous devices in such systems may easily be replaced by devices with higher data rates without impacting the interconnect design." (Page 85,

lines 5-8). This is clearly not possible with Venkataraman because, if node components were replaced with components having higher data rates, the synchronization with the clock rate of crossbar unit 30 would necessarily be affected.

None of the teachings of MacWilliams and Powell cure the deficiencies of Venkataraman discussed above. Therefore, in view of the foregoing, the rejection of claim 1 over the combination of Venkataraman, MacWilliams, and Powell is believed overcome for at least the reasons discussed. Similarly, the rejection of any claims depending from claim 1 either directly or indirectly are believed overcome for at least these reasons.

The Applicants respectfully acknowledge the Examiner's indication of allowable subject matter in claims 2-10, 14, 16, 17, 25, 26, 28, and 30. However, in view of the foregoing, the Applicants believe these claims to be allowable in their current condition without amendment.

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested. If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (510) 663-1100.

Respectfully submitted,
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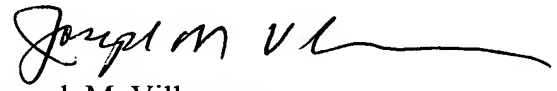

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